REMARKS/ARGUMENTS

In response to the Examiner's final Office Action of May 13, 2008 issued with respect to the present RCE application, the Applicant submits the following Remarks.

Regarding 35 USC 112, first and second paragraph Rejections

It is respectfully submitted that the subject matter of pending independent claim 1, and claims 3-6 dependent therefrom, is enabled by the description of the present specification and is clear, for at least the following reasons.

Firstly, it is noted that the Applicant erroneously cited the disclosure from the specification and drawings as originally filed in the Applicant's previously submitted Remarks. It is respectfully submitted that the Applicant should have referred to the substitute specification and drawings filed July 21, 2005, to which the Applicant now refers in the following arguments. The Applicant apologizes for any inconvenience caused by this error to the Examiner.

Substitute Fig. 28 illustrates the QA chip (e.g., the claimed integrated circuit) as having an analogue unit which outputs the clock signal SysClk to the logic circuitry (e.g., central processing unit, memory interface unit, ID unit, etc.) of the chip. Substitute Fig. 29 illustrates the analogue unit as including a ring oscillator for generating the clock signal, as described at page 49, lines 10-32 of the substitute specification.

Thus, from the disclosure at page 49, lines 10-32 of the substitute specification and Figs. 28 and 29 of the substitute drawings, it is clear that the on-board system clock is output to logic circuitry of the integrated circuit, as recited in the claimed invention.

Further, substitute Fig. 38 illustrates the ring oscillator as including a clock filter, with associated temperature sensor, which is connected between the ring oscillator circuit and divider circuit Div5 for allowing the clock signal from the ring oscillator circuit through to the divider circuit only when the temperature range is such that the chip can function correctly, as is described at page 45, line 8-page 46, line 4 and page 56, lines 1-21 of the substitute specification.

Thus, in combination with the above cited disclosure and drawings, from the disclosure at page 45, line 8-page 46, line 4 and page 56, lines 1-21 of the substitute specification and Fig. 38 of the substitute drawings, it is clear that the integrated circuit has a clock filter which prevents output of the system clock when certain temperature conditions are met.

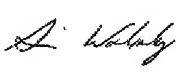
35 USC 102(e) and 103(a) Rejections

It is respectfully submitted that the subject matter of amended independent claim 1, and claims 4-6 dependent therefrom, is not disclosed or suggested by any one or more of Uchida, Yamazaki, Chemla and Kitano, for at least the above discussed reasons and those previously submitted by the Applicant.

It is respectfully submitted that all of the Examiner's rejections have been traversed. Accordingly, it is submitted that the present application is in condition for allowance and reconsideration of the present application is respectfully requested.

Very respectfully,

Applicant/s:



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